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Next – generation interdigitated back-contacted silicon heterojunction solar cells and modules by design and process innovations



NextBase - Deliverable report

D5.3- IBC-SHJ device with efficiency $\geq 26.0\%$ on 6-in wafer

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List of acronyms, abbreviations and definitions

Table 1. Acronym table

Abbreviation	Explanation
ARC	Anti-reflection coating
α-Si:H	Hydrogenated amorphous silicon
c-Si	Crystalline silicon
Eff.	Conversion efficiency
FF	Fill factor
IBC	Interdigitated back contact
ITO	Indium tin oxide
J_{sc}	Short-circuit current density
nc-Si:H	Hydrogenated nano-crystalline silicon
R_{series}	Series resistance
SHJ	Silicon heterojunction
SiNx	Silicon nitride
TCO	Transparent conductive oxide
V_{oc}	Open-circuit voltage

1 Introduction

D5.3 provides a status of the champion IBC-SHJ devices processed in the frame of NextBase. The final IBC-SHJ architecture – featuring a tunnelling electron contact – is presented, as well as its process flow with a single PECVD patterning step via shadow mask. The best demonstrated efficiencies with this approach are of 25.4 % on 25 cm² FZ wafer, and of 25.35 % on 92 cm² Cz wafer. A loss analysis explaining the deviation to the targeted 26.0 % efficiency is provided, and the path to achieve higher efficiency is discussed.

Deliverable Number	Deliverable name	Lead partner	Type	Dissemination level	Due date
D5.3	IBC-SHJ device with efficiency $\geq 26.0\%$ on 6-in wafer	CSEM	DEM	PU	M36

1 NextBase’s champion IBC-SHJ devices

Figure 1 plots the evolution of the efficiency of the IBC-SHJ champion devices obtained using the different patterning techniques and associated process flows under investigation in WP5 (see D5.1 report for details) during the whole duration of the NextBase project.

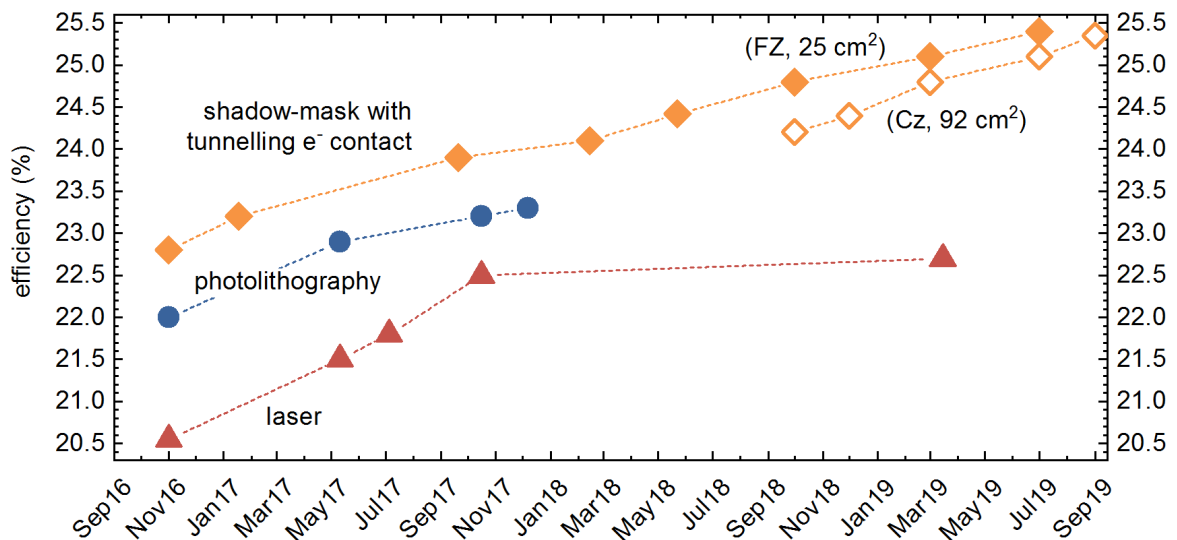
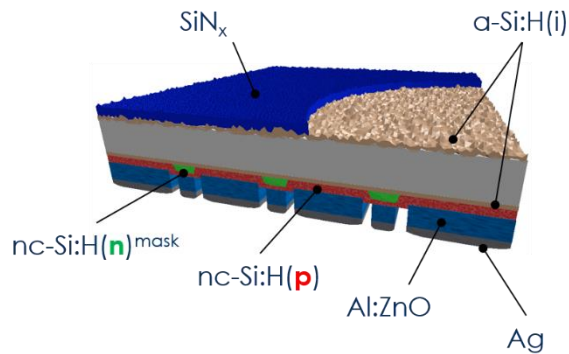


Figure 1. Evolution of the efficiency of the champion devices for each patterning technique under investigation in WP5 during the NextBase project.

As can be seen, even if regular progresses were recorded with all investigated patterning schemes, the efficiencies are eventually topped by IBC-SHJ devices processed using the combination of shadow mask as a patterning technique and a tunnelling electron contact [1]. The architecture of these devices is depicted in Figure 2, and their process flow in Figure 3. Such devices demonstrated efficiencies close to 25.5 % both on 25 cm² FZ wafers and on 92 cm² Cz wafers. Note that the transfer of this technology on full M2 Cz wafers is ongoing and already reached 24.25 % efficiency. Figure 4 below presents the full I-V curves of these best devices.

Remarkably, note that this approach – combining shadow mask patterning with a tunnelling electron contact – allows to reach > 25 % efficiency with only 9 process steps, probably making it one of the leanest process flows for IBC-SHJ devices.



n-type wafer preparation

- 1) Texturing & cleaning

Surface Passivation

- 2) Front a-Si:H(i)
- 3) Rear a-Si:H(i)

Tunnel junction

- 4) Rear localized nc-Si:H(n)
- 5) Rear full nc-Si:H(p)

ARC and contacts

- 6) Front SiNx
- 7) Rear Al:ZnO

Metallization & opening

- 8) Screen-printed Ag
- 9) Wet etching

Cell Sorting

- 10) IV measurement

Figure 2. Architecture of an IBC-SHJ device with tunnelling electron contact.

Figure 3. Process flow of IBC-SHJ devices with tunnelling electron contact patterned via shadow mask.

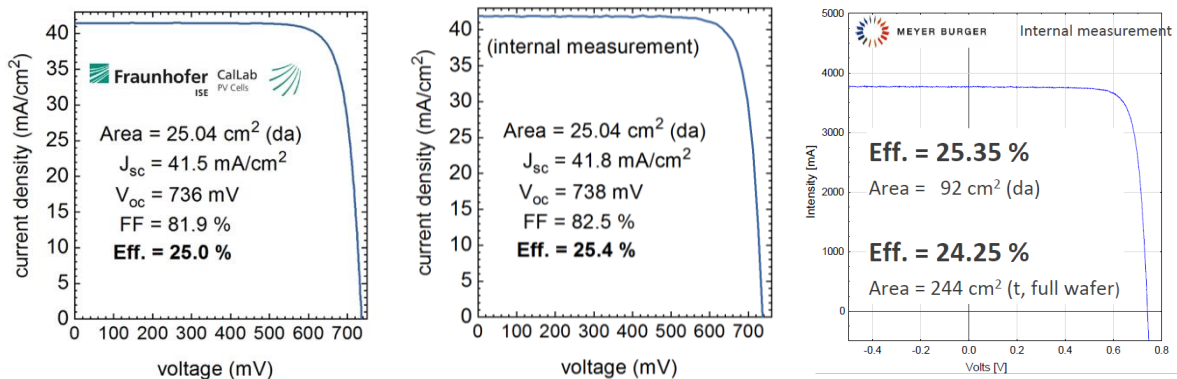


Figure 4. Champion IBC-SHJ devices obtained in the frame of NextBase.

2 Loss analysis & roadmap towards higher efficiency

In spite of the impressive results presented in Section 1 above, the highest demonstrated efficiency falls short to the 26.0 % value targeted in NextBase. Table 2 below compares the key performance indicators for the 25.4 % efficient IBC-SHJ device (presented in Figure 4 middle) to those required for a 26.0 % efficient device.

Table 2. Comparison of the key performance indicators for the 25.4 % efficient IBC-SHJ device (presented in Figure 4 middle) to those required for a 26.0 % efficient device.

	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	Eff. (%)
26.0 % target	42.0	730	85	26.0
25.4 % NextBase's best device	41.8	738	82.5	25.4

As can be seen from Table 2, the J_{sc} of the champion device falls a bit short to the 42.0 mA/cm² target, but this small loss is entirely compensated by the over-performing V_{oc} of the NextBase's champion solar cell (738 mV vs. an anticipated value of 730 mV). In contrast, the major reason for the final efficiency to fall short to the 26.0 % targeted value is to be found in the FF value, which is 2.5 %_{abs} lower than the targeted one. To explain the reasons for this deviation, Figure 5 plots the R_{series} loss analysis of our champion device using the latest series resistance modelling for IBC-SHJ devices [2].

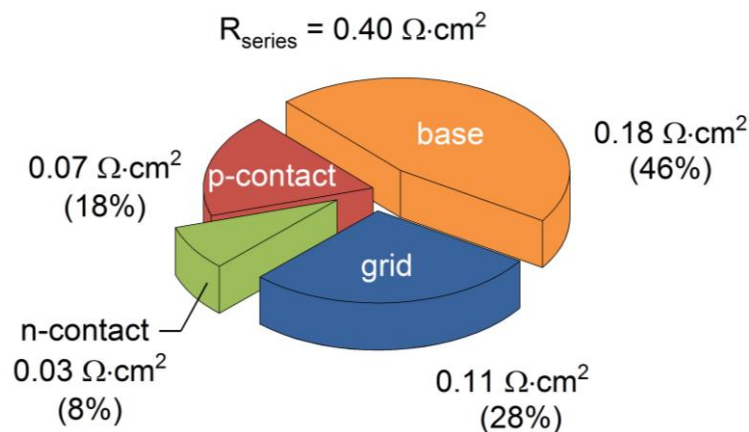


Figure 5 clearly pinpoints that the major contribution to the overall R_{series} of our IBC-SHJ champion device lies in the lateral base resistance owing to the 2.5 mm pitch currently used in this best device. Numerical simulations performed in WP8 already provided the reduced pitch values expected to unlock the path to higher FF values (see D8.5 report). Their practical implementation into IBC-SHJ devices is ongoing, but is yet hindered by technical challenges.

3 Conclusion & outlook

This deliverable reports on the champion IBC-SHJ solar cells demonstrated in the frame of NextBase. Up to 25.4 % efficiencies were demonstrated on 25 cm² FZ wafers and on 92 cm² industrial Cz wafers. These results are the European record to date for such solar cells technology. The path towards even higher efficiency has been clearly identified – especially regarding the need to mitigate the lateral transport losses – and the technological building blocks required to reach this goal are under development.

4 References

- [1] A. Tomasi *et al.*, “Simple processing of back-contacted silicon heterojunction solar cells using selective-area crystalline growth,” *Nat. Energy*, vol. 2, no. April, p. 17062, 2017.
- [2] D. Lachenal *et al.*, “Optimization of tunnel-junction IBC solar cells based on a series resistance model,” *Sol. Energy Mater. Sol. Cells*, 2019.