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Next – generation interdigitated back-contacted silicon heterojunction solar cells and modules by design and process innovations

NextBase - Deliverable report

D4.1- IBC devices employing a-Si:H- and µc-Si:H-based contact stacks with Voc > 740 mV and FF > 82%

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Publishable summary

This deliverable consists of demonstrating a device with Voc > 740 mV and FF > 82%, in a device employing a-Si:H- and µc-Si:H-based contact stacks. It is related to task 4.1, focusing on the development of such contact stacks. A Voc > 740 mV (namely 741 mV) could be obtained, however best FF was 81.2% (together with a Voc of 734 mV, Jsc of 41.7 mA/cm^2 for an efficiency of 24.8%). This best device lies therefore 1% short in terms of both Voc and FF compared to the target values. This shortcoming is analysed in details in this report. Main conclusions are that the losses associated with the resistance of the contact stacks are low enough to allow a FF up to 85%, yet other losses related to sub-optimal wafer thickness and doping, as well as imperfect passivation and sub-optimal rear-contact pitch are the main remaining losses to tackle. Comparing the 81.2% demonstrated FF to an ideal FF of 89.1%, these losses represent altogether 7% (abs.) (that is 86% (rel.) of the total loss) whereas the contact stacks and metallization are responsible for only 1.1% (abs.) FF loss (that is 14% (rel.) of the total loss). Tackling these other losses will therefore be the focus in future activities to further improve the FF of IBC devices developed within NextBase.

Contents

List of acronyms, abbreviations and definitions

Table 0.1 Acronym table

Abbreviation	Explanation
***a*-Si:H**	Hydrogenated amorphous silicon
FF	Fill factor
IBC	Interdigitated back contact
Jsc	Short-circuit current density
mA/cm^2	milliampere per square centimeter
***µc*-Si:H**	Hydrogenated micro-crystalline silicon
PECVD	Plasma-enahnced chemical vapour deposition
PVD	Physical vapour deposition
SHJ	Silicon heterojunction
TCO	Transparent conductive oxide
V_{oc}	Open-circuit voltage

1 Introduction

The goal of WP4 is to develop the layers for high-efficiency IBC. This deliverable is an intermediate step to ensure that the team is on track towards the high-efficiency devices to be demonstrated at the end of the project. In particular, it aims at demonstrating that contact layers to extract charges from ultra-efficient IBC devices with minimal electrical losses are available.

It has a component on open-circuit voltage (Voc) and fill factor (FF). The first one gives an indication on the quality of the passivation of the wafer. A high Voc ensures that electrical charges generated by sunlight do not get lost for electricity generation due to electronic defects. The second one gives (additionally to the passivation quality) an indication on the electrical losses upon extracting the charges, typically analysed in terms of a series resistance.

The target values of 740 mV of Voc and 82% of FF are very aggressive and would allow, assuming a realistic Jsc of 42.7 mA/cm^2—already demonstrated within NextBase, see D4.3—to reach a 25.9%-efficient device, very close to the final project goal of 26%.

Deliverable Number	Deliverable name	Lead partner	Type	Dissemination level	Due date
D4.1	IBC devices with a-Si:H and µc-Si:H based contact stacks with Voc > 740 mV and FF > 82%	EPFL	DEM	CO	M24

1 Results obtained towards this deliverable

The highest-efficiency device result achieved so far is shown in **Figure 1**. It combines a very high FF of 81.2% and Voc of 734 mV. The silicon heterojunction technology is especially famous for demonstrating record-high Voc values, but reaching values above 80% is specifically arduous for such devices [1], [2]. The combination of excellent Voc and FF in a single device is therefore a great achievement.

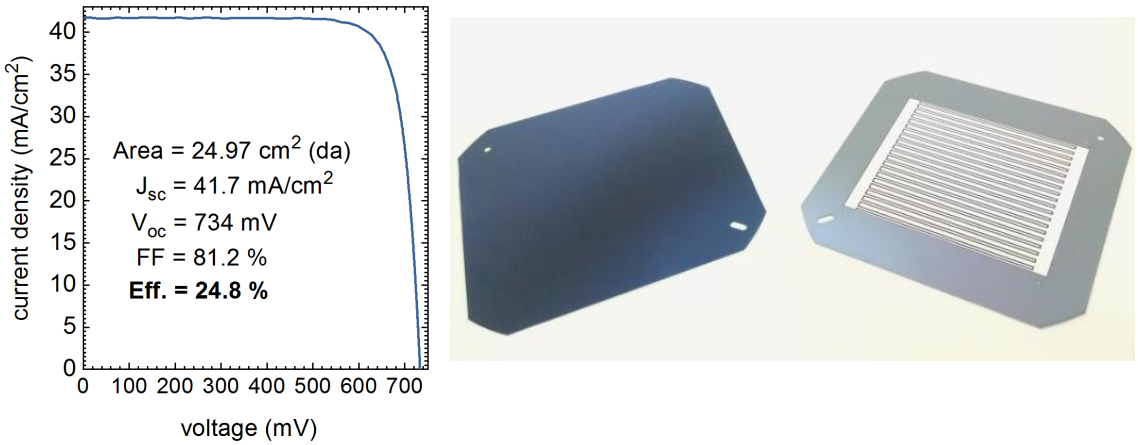

Figure 1. left: IV curve and main IV parameters of the best-FF device produced in WP5 using Si-based layers developed in WP4. Right: photograph of such solar cell, front and rear, the size of the pseudosquare wafer is 80 mm x 80 mm.

Compared to the ambitious deliverable targets, it falls short by less than 1% in both aspects. The origin of the losses incurring to this device are depicted further down, yet it should be noted on the up-side that this results was obtained :

- on a relatively large-area device (25 cm^2),
- using industry-relevant tools and processes (surface preparation, PECVD depositions, PVD depositions, screen printing metallization),
- using industry-relevant patterning technique (shadow mask / screen printing) without photolithography or back etch of silicon layers.

The remarkable efficiency of 24.8% with such simple process places the Nextbase consortium in a very favourable situation to reach the 26% efficiency target on cell level (task led by WP5) by the end of the project. Besides, these processes are the ones being upscaled further to industrial production (task led by WP6), making the overall objectives of a 22%-efficient module appear very much within reach for the cell aspects.

In the following part of this short report, a discussion on the reasons for the shortcomings of the FF is given.

2 Loss analysis for the shortcoming towards this deliverable

Voc considerations

For the wafer thickness and doping used in the best device presented in Figure 1, (thickness around 240 µm and resistivity around 3 Ohm.cm), the Voc is intrinsically limited to 745 mV [3]. This wafer thickness is practical for manipulation in the lab but suboptimal for device efficiency, since it has been shown that thicknesses around 100 µm would allow for the highest performances. Indeed, applying a similar process as used for the device from Figure 1 to a thinner wafer (~100 µm), a Voc of 741 mV was obtained. Process changes in the PECVD recipe of the doped layers made the FF lower than 80% though. This confirms that a Voc reaching the target value of 740 mV is within reach provided a suitable combination of doping and thickness of the wafer is chosen.

FF considerations

Figure 2 shows a detailed waterfall analysis of the FF losses performed on the best-performing device at M18, showing a FF of 79.6%, as well as the same waterfall for the most recent best-FF device and the targeted waterfall to reach the realistically highest FF.

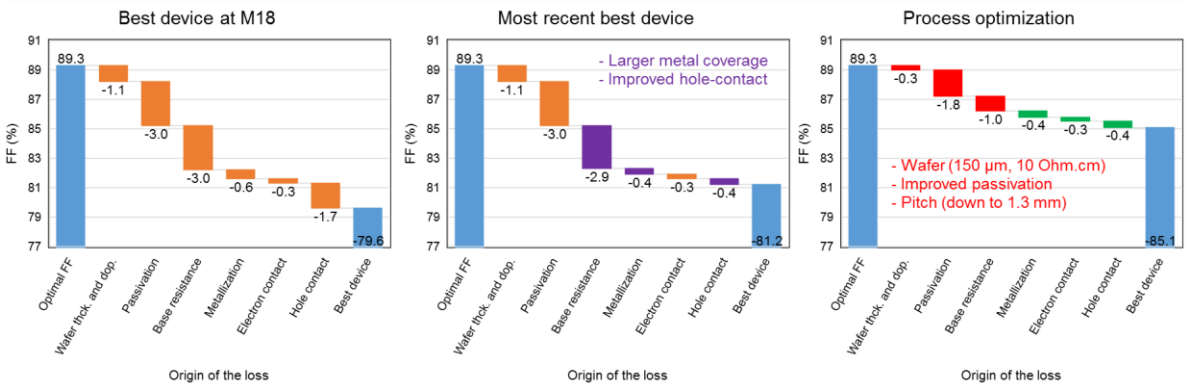

Figure 2. *Waterfall diagram of the losses identified between the best-FF device at M18, the most recent best device, and the targeted improvements until the project end. Such 85% FF would allow a 26%-efficient device combined to the Voc and Jsc of the present-best device.*

Wafer thickness and doping: Similarly to Voc, the chosen wafer thickness and doping does not correspond to the optimal one [3], and 1.1% FF are lost this way. At this stage it seems relevant to justify this sub-optimal choice: one of the reason is that thicker wafers (as are used in our case with 240 µm) provide higher current due to the better absorption of infrared light. Optimal wafer thickness taking into account practical life constraints was identified to be slightly thicker than the theoretical optimal, and in the range of 140 µm [2],

[4]. Furthermore, and most relevant in our situation of laboratory devices, repeated manual handling of the wafers can lead to a high breakage rate for thin wafers, making thicker wafers more practical to use. Note that this is not the case in an industrial production line where recent progress of the automation made it possible to use ~140 µm-thick wafers with a very high yield. This practical reason, together with the fact that the FFs reached by different partners in the consortium were so far mostly limited by other losses, made the choice of a thicker wafer preferable so far. In the last year, though, the switch to thinner wafers will be progressively made to ensure that highest efficiency can be harvested.

Passivation: As was mentioned by Yoshikawa et al. and discussed in detail by Haschke et al., excellent surface passivation is mandatory to reach a high FF. In spite of the excellent passivation reached in the consortium (especially after initial passivation), losses are still present, accounting for a 3% total loss. This can be ascribed to damage to the samples during multiple handlings, or to the harsh processing conditions of the contact layers (PECVD of the p µc-Si:H layer typically) and rear-side electrode (consisting of a reactively-sputtered transparent conductive electrode and screen-printed silver metallization). Particular care to prevent any scratch or damage to the surface, together with process optimization of these final steps would be required to further improve this part. In a recent experiment, the passivation-limited FF was 85% (with an intrinsic wafer-limited FF of 88%), then after contact formation it dropped to 84%, then after multiple handling and electrode fabrication it dropped to 81%. This led to a final FF of 77% when accounting for the other losses (due to series resistance). With a loss-free processing, a FF of 81% would have been reached. This was the case for the best-efficient device (85% of passivation-limited FF throughout all processing).

Base resistance: Since the Nextbase project focuses on interdigitated back contacted devices, charge extraction for both polarities occurs in adjacent contact stripes with alternating polarity on the rear side. Positive and negative charges, generated in the whole volume of the wafer, thus have to travel laterally in the wafer itself to reach the electrode of the appropriate polarity. This incurs resistive losses directly impacting FF. To mitigate this, the finest possible pitch shall be chosen to reduce the distance to travel before reaching the suitable electrode. Practical aspects (lithography-free alignment, tapering during deposition through shadow mask, mechanical robustness of the masks, …) limit the pitch to larger dimensions. Tuning of the wafer doping (towards higher doping) can also mitigate this loss, yet Voc and passivation considerations tend to favour lower doping, leading to an overall compromise. This aspect is to be improved in future designs, based on inputs from simulation (WP8).

Metallization: as shown in Figure 1, fingers lead to a busbar at the edge of the active area, and some losses are present to collect current from all along the fingers to the busbar due to the finite thickness and conductivity of the silver paste employed.

Electron contact and Hole contact: One major cause of resistance loss in heterojunction is the extraction of electrical charges from the wafer to the electrode which is commonly referred to as contact resistance. Since the IBC design allows collection of charges of both polarities on one single side (the rear side), this cause for resistance loss is roughly doubled. Fortunately, the contact design can be adjusted to allow a larger fraction of the area to collect the most lossy type of charge (typically holes) whereas the collection of the other one (typically electrons) is restricted to a lower fraction. This has been discussed in D8.1 (M12). Additionally, contrary to standard 2-side contacted devices, blue and visible light parasitic absorption in the contact layers is not an issue, relaxing a constraint in terms of thickness or material type. Relatively thick, low-bandgap, µc-Si:H doped layers are typically used in the best IBC devices used here, whereas such layer would prohibitively absorb short-wavelength light should it be used on the light-incoming side of a standard device.

Overall, FF losses related to contact-layers (the last two items of the waterfall diagram) already reach the final target values in the present-best device. This indicates that T4.1 effort was fruitful and delivered the necessary outcome. Further FF improvements will mostly be tackled in WP5 with pitch modification, change of wafer thickness, and process optimization to reach outstanding passivation.

3 Risks and interconnections

3.1 Risks/problems encountered

The main encountered problem was related to the reaching of an 82%-FF device, which does not only rely on work related to WP4 but also to WP3 (wafer quality) and WP5 (patterning scheme) amongst others. Due to the steady progress and reaching of targets in due time in WP3 and WP5, this had only a minor impact on the achievement of this deliverable, and a shortcoming of less than 1% was observed.

3.2 Interconnections with other deliverables

This deliverable is related to the following deliverables/milestones/tasks:

- Deliverables
  - D5.1: “Selection of suitable patterning schemes for > 26%-efficient devices.”
  - D5.3: “IBC device with efficiency > 26% on 6-inch wafer.”
- Milstones
  - 4: “Selection of most suitable front stack and back contact system.”
  - 5: “Demonstration of an IBC-SHJ device on 6-inch wafer with the most promising processes for patterning and light trapping.”
- Tasks
  - 4.1: “Novel FSF and passivation materials for the front side of IBC-SHJ devices.”
  - 5.3: “Processing of IBC-SHJ devices with with efficiency > 26%.”

4 Conclusion and next steps

Although this deliverable is only partly achieved, one of the targeted value was demonstrated (Voc > 740 mV) and the other falls short by less than 1% (FF of 81.2% vs. 82%). A waterfall diagram was produced to detail the reasons for this shortcoming. Main FF losses for this best-FF device lie in the imperfect passivation, sub-optimal wafer thickness and doping, and sub-optimal pitch. These are currently being tackled in WP5. On the other hand, the FF losses related to T4.1 are already reaching the target values allowing an 85% FF which would ease the constraints on Voc and Jsc for the final 26%-efficiency target. This result is therefore still very valuable considering that it was obtained using simple process steps that are being transferred to WP5 and WP6 for the industrialization of this technology. It is notable that the highest-efficiency device produced in WP5 using learnings from tasks associated to this deliverable is showing a remarkable combination of 734 mV of Voc and 81.2% FF, all demonstrated with the simplest patterning scheme under investigation and on a 25-cm^2 area. When devices reaching the target of this deliverable are measured, an update will be given.

5 References

[1] S. De Wolf, A. Descoeudres, Z. C. Holman, and C. Ballif, “High-efficiency silicon heterojunction solar cells: A review,” *Green*, vol. 2, no. 1, pp. 7–24, 2012.

[2] J. Haschke, O. Dupré, M. Boccard, and C. Ballif, “Silicon heterojunction solar cells: Recent technological development and practical aspects - from lab to industry,” *Sol. Energy Mater. Sol. Cells*, vol. 187, pp. 140–153, Dec. 2018.

[3] A. Richter, M. Hermle, and S. W. Glunz, “Reassessment of the Limiting Efficiency for Crystalline Silicon Solar Cells,” *IEEE J. Photovoltaics*, vol. 3, no. 4, pp. 1184–1191, 2013.

[4] K. Yoshikawa *et al.*, “Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%,” *Nat. Energy*, vol. 2, no. 5, p. 17032, Mar. 2017.