EUROPEAN COMMISSION

HORIZON 2020 PROGRAMME
TOPIC H2020-LCE-07-2016-2017
Developing the next generation technologies of renewable electricity and heating/cooling

GA No. 727523

Next – generation interdigitated back-contacted silicon heterojunction solar cells and modules by design and process innovations

NEXTBASE
THE NEXT GENERATION BASELINE

NextBase - Deliverable report

D3.3 – Textured c-Si exhibiting low reflectance (< 5%) and implied current density beyond 41.5 mA/cm^2

Deliverable No.	NextBase D3.3	
Related WP	WP3	
Deliverable Title	Textured c-Si exhibiting low reflectance (<5%) and implied current density beyond 41.5 mA/cm^2	
Deliverable Date		
Deliverable Type	Report	
Dissemination level	Public (PU)	
Author(s)	Paul Procel (TUD), Hariharsudan Sivaramakrishnan Radhakrishnan (imec)	09-2018
Checked by	Olindo Isabella (TUD)	06-09-2018
Reviewed by (if applicable)	EB members	20-09-2018
Approved by	Kaining Ding (Jülich) - Coordinator	25-09-2018
Status	Final	

Disclaimer/ Acknowledgment

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 727523. The information and views set out in this publication does not necessarily reflect the official opinion of the European Commission. Neither the European Union institutions and bodies nor any person acting on their behalf, may be held responsible for the use which may be made of the information contained therein.

Publishable summary

An evaluation of modulated surface texturing (MST) is carried out by comparing the optical properties and passivation quality with the standard random pyramids texturing (RPT) scheme. MST is deployed by applying nano-cones on top of RPT, thus resulting in anti-reflective (low-reflectance) features. By combining MST scheme (for less front surface reflectance losses) with IBC technology, a high J_{sc} is expected. Moreover, with such a texture, there is no necessity to use an additional anti-reflection coating layer during device fabrication. However, nano-featured surfaces also entails a more defective interface due to applied processes that damage the interface. Then, two concurrent conditions are the core to achieve implied short circuit current > 41.5 mA/cm^2: improved light-trapping scheme and also good passivation.

Nano texturing process is carried out by reactive ion etching with a mixture of SF_6 and O_2 gases. After achieving the nano-roughness reaction (oxidation and etching), the minimum etching process time to reach almost a perfect light-in coupling is estimated.

Afterwards, using the optimized process, optical properties evaluation is performed by a comparison of spectral reflectance of MST and RPT samples. Before lamination, results showed that the reflection losses can be reduced by up to 3.4 mA/cm^2. After lamination, this advantage is reduced to 1 mA/cm^2. In general, MST samples exhibited front reflection losses below 4% and also the highest implied photocurrent beyond 41.5 mA/cm^2 even after encapsulation without any ARC.

Finally, to include MST process on IBC-SHJ devices, the passivation quality of MST interfaces using i-a-Si:H was investigated in terms of effective lifetime. Plasma conditions were adjusted to achieve a conformal i-a-Si:H layer leading to effective lifetime beyond 500 µs. Then, the effect of defect removal etching (DRE) time on effective minority carrier lifetime was evaluated. MST with 60 s DRE time exhibits promising effective lifetime values of 1.2 ms and 715 mV iV_{oc}, thus demonstrating good passivation (low recombination) even on nano-rough surfaces. Such DRE time demonstrates insignificant variation on front reflectivity losses when compared with 15s and 30 s DRE time. Hence, MST with 60 s DRE concurrently exhibits reduced reflectivity losses and recombination losses anticipating the potential of MST to achieve J_{sc} > 41.5 mA/cm^2 in device level.

Contents

List of acronyms, abbreviations and definitions

Table 1.1 Acronym table

Abbreviation	Explanation
***i*-*a*-Si:H**	Intrinsic hydrogenated amorphous silicon
IBC	Interdigitated back contact
Jsc	Shor circuit current
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
iVoc	Implied open circuit voltage
λ	Wavelength
MST	Modulated surface texture
b-Si	Black silicon
c-Si	Crystalline silicon
RIE	Reactive ion etching
DRE	Defect removal etching
PECVD	Plasma enhanced chemical vapour deposition
RPT	Random pyramid texture
KOH	Potassium hydroxide
QSSPC	Quasi-steady-state photo-conductance

1 Introduction

Deliverable D3.3 is related to task 3.4, which aims at the development of advanced wafer texture consisting of nano-scale textures on micro-scale texture to improve the light-management of the optical system. Nano-texturing scheme provides almost ideal light in-coupling but not an efficient light scattering. Micro-texturing approach affords almost perfect Lambertian scattering. Combining nano- and micro-texturing surfaces, it is possible to achieve almost ideal light in-coupling and light scattering by means of modulated surface texturing (MST) (Ingenito, Isabella, & Zeman, 2015). Thus, applying such a concept and depending on passivation, implied photocurrent beyond 41.5 mA/cm^2 is potentially attainable without an anti-reflection coating. Moreover, this approach allows to mitigate the optical losses if wafer's rear side is flat, thus enabling more flexibility on IBCs contact patterning (Ingenito et al., 2015).

Although nano-texturing surfaces improves light-trapping, it entails a more defective interface due to applied processes that damage the interface. Accordingly, two concurrent conditions are the core to achieve implied short circuit current > 41.5 mA/cm^2: improved light-trapping scheme and also good passivation. For advanced wafer texture, these two competitive mechanisms are analysed in terms of reflectance in case of light-trapping and lifetime in case of recombination.

D3.3 summarises the results achieved to reach advanced texturing and its evaluation by comparing the optical properties and passivation quality with the standard random pyramids-texturing approach.

Deliverable Number	Deliverable name	Lead partner	Type	Dissemination level	Due date
D3.3	Textured c-Si exhibiting low reflectance (< 5 %) and implied current density beyond 41.5 mA/cm^2	TUD	R	PU	M24

2 Evaluation of Modulated surface texture (MST)

For this evaluation, 2-5 Ω·cm 4-inch <100> n-type FZ c-Si wafers were used. Micro-texturing process consists of wet alkaline etching producing randomly distributed micro-pyramids. Nano-texturing process is carried out by mask-less reactive ion etching (RIE) tool using a gas mixture of SF_6 and O_2. In order to achieve MST surface, micro texturing process is initially applied followed by a nano-texturing process. Scanning electron microscopy (SEM) images in Figure 1 illustrate the MST concept.

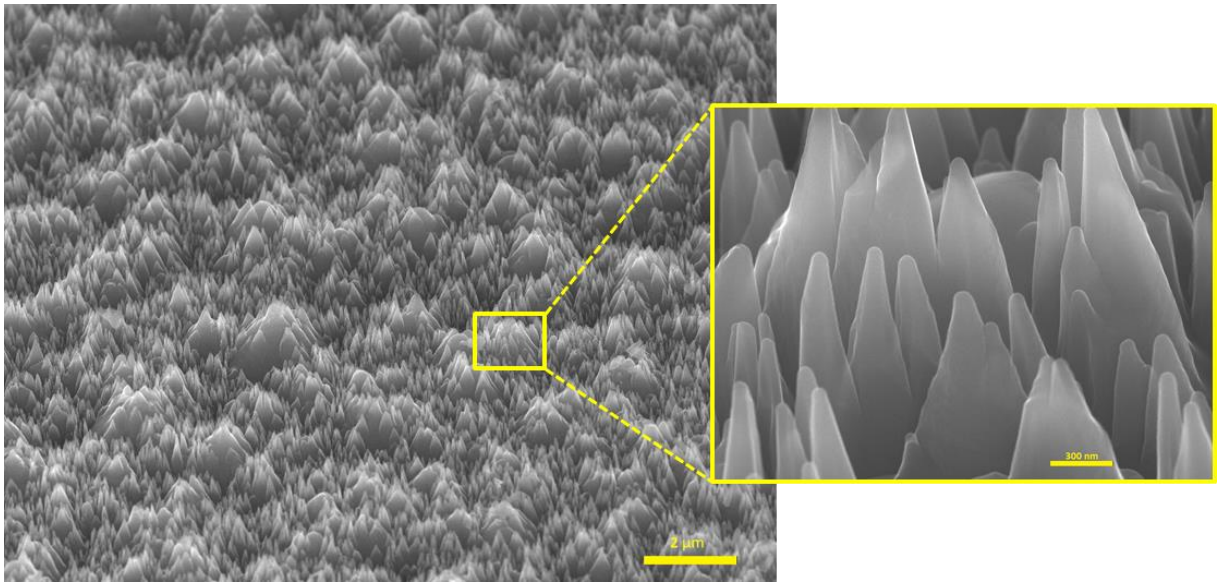


Figure 1. SEM images for MST surface morphology (Procel et al., n.d.).

2.1 Nano-texturing process optimization

Based on RIE premises, nano-texturing process consists of a combination of two reactions: i) surface oxidation and ii) ion etching. These two mechanisms work in anisotropic regime to form nano-cones at c-Si interface. Fluorine radicals etch the c-Si interface while the oxygen radicals passivate the surface (Jansen, Gardeniers, & De Boer, n.d.), thus leading to nano-features surface. Such a special plasma regime is achieved following the process suggested in (Jansen et al., n.d.). Once nano-texturing (black silicon, b-Si) regime is achieved, the process is optimized aiming at a fast etching process concurrently with minimal reflectivity losses. To this purpose, the evaluation is carried out on polished (flat) interfaces to study only the effect of nano-texturing process as Figure 2 illustrates.

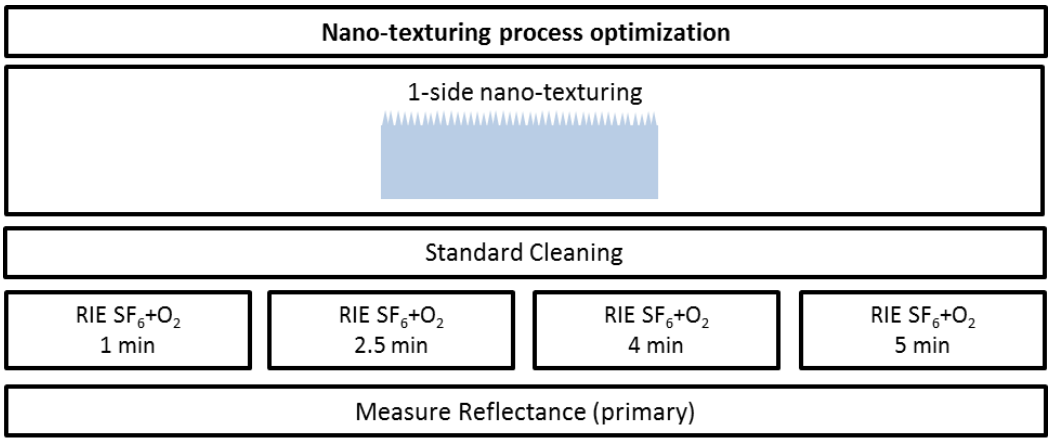


Figure 2. Experimental matrix to evaluate the optimal time to create nano-texturing from RIE. Minimize primary reflectance is used as indicator for optimal time.

Accordingly, different process times were evaluated (Figure 2**Error! Reference source not found.**) in terms of reflectance curves shown in and confirmed by calculating aspect ratio A_R from SEM images in Figure 3. As Figure 3 reports, after one minute etching A_R is around 3 leading to relatively high reflectance (black curve), as early stage of b-Si and nano-cones features are not complete. A_R larger than 5 is achieved after 2.5 min of etching, however reflectance revealed that process is not completely anisotropic, since some flat surface is observed on the bottom of nano-needles. After 5 min etching time c-Si interface is completely covered by nano-cones and minimum reflectance is achieved. Therefore, 5 minutes etching time is considered as the optimal time to reach minimized reflectivity losses.

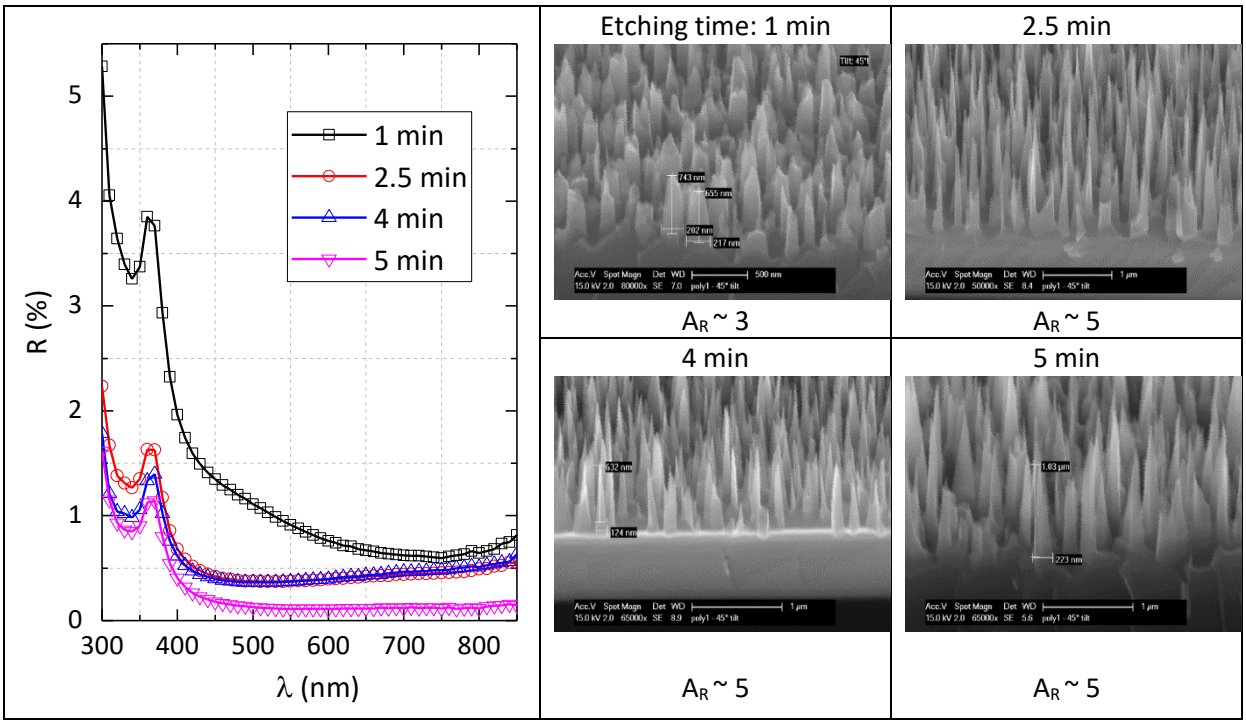


Figure 3: *Left: Reflectance evaluation for different nano-cones etching time. Right: SEM images revealing A_R and surface etching for different etching time. For 1 min, surface is not completely etched and nano-cones exhibits AR ~ 3. For 2.5 min AR is around 5, but surface is not complete etched. For 4 min, the surface is not completely etched yet, but, for 5 min, c-Si interface is completely covered by nano-cones with AR ~ 5.*

2.2 MST optical evaluation

The optical performance of MST is bench-marked against the standard random pyramids texturing scheme. The experimental split matrix for this evaluation is depicted in Figure 4.

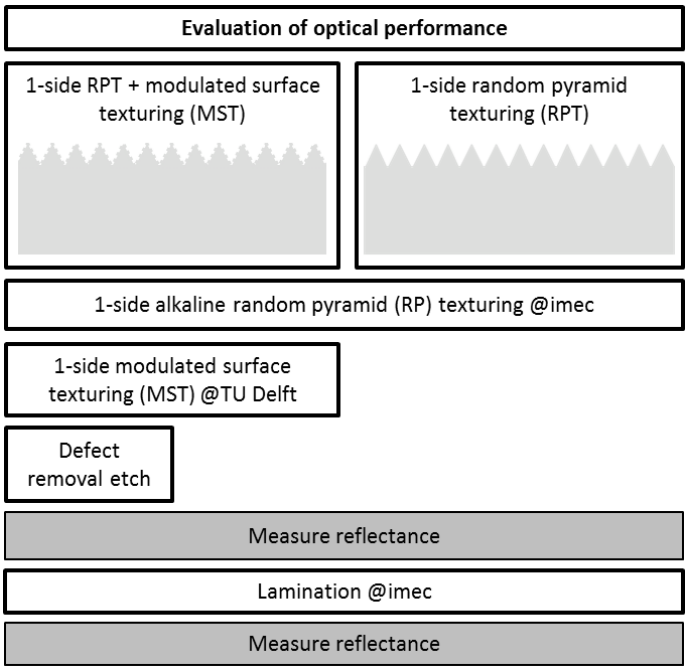


Figure 4. Experimental split matrix to evaluate the optical performance of samples with modulated surface texture (MST) before and after lamination, in comparison to standard random pyramids surface texture.

Following a wet chemical cleaning step, a 40 nm-thick thermal oxide layer was grown on both surfaces of the wafers, using thermal oxidation at 975°C. Subsequently, the oxide layer on 1 side of the wafers was removed selectively using vapour HF treatment. The oxide layer remaining on one of the sides of the wafers acts as a masking layer during texturing, enabling single-side texturing of these wafers. The texturing was performed in a KOH solution at 80°C to produce random pyramids texture on the thermal oxide-free surface of the wafers.

Some of the wafers then received MST process with nano-cones on top of the random pyramids. Following a wet chemical surface clean, some of MST wafers were subjected to a short defect-removal etch (DRE) for 30 s, based on diluted Tetramethyl ammonium hydroxide (TMAH) (Ingenito et al., 2015). DRE is typically needed to achieve a low surface recombination velocity after passivation. This results in 3 splits of wafers with:

- Random pyramids texture (RPT) only
- RPT + modulated surface texture (MST)
- RPT + MST with a defect-removal etch (DRE).

The spectral reflectance of these wafers is measured in the wavelength range of 250 nm to 1200 nm using an optical spectrometer. Subsequently, the wafers are laminated with a Borealis encapsulant between a flat front glass and a white back-sheet. Once again, spectral reflectance in the same wavelength range is measured to evaluate their performance after lamination.

The reflectance as a function of wavelength, measured on the different surfaces, before lamination, is plotted in Figure 5 (a). Before lamination, the wafers with only random pyramids surface texture exhibit a rather typical reflectance of < 12% in the wavelength range of 600 nm to 1000 nm. Note that the reflection losses in the short wavelength range are due to direct front reflection loss while those in the long wavelength range (> 1000 nm) are mainly due to light reflecting from the back-side of the wafer and escaping through the front surface.

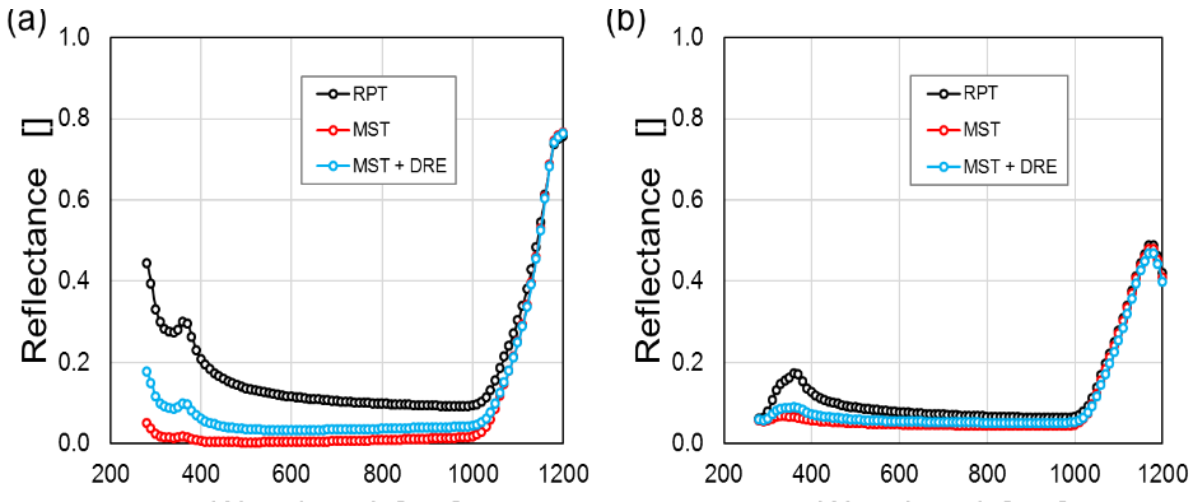


Figure 5. Reflectance as a function of wavelength measured on samples with different surface structures, namely random pyramids texture (RPT), modulated surface texture (MST) and MST with defect-removal etch (DRE), (a) before lamination and (b) after lamination.

Before lamination, the MST clearly outperforms the random pyramids surface texture, with a broad-band low-reflectance of < 2% for the entire wavelength range from 300 nm to 1000 nm, demonstrating the superior optical light in-coupling and light trapping of the MST. Thus, with the MST, no additional anti-reflection coating is needed. The short defect-removal etch does have a negative impact, whereby the reflectance at all wavelengths is increased slightly, especially below 400 nm. Nevertheless, in the range of wavelengths from 450 nm to 1000 nm, the reflectance is still < 4%, which is still much better compared to random pyramids surface texture.

The spectral reflectance, measured on the same samples after lamination, is plotted in Figure 5 (b). In this case, the differences in the reflectance between different samples are less significant. Nevertheless, in comparison with random pyramids surface texture, the MST samples still show a lower reflectance throughout the entire wavelength range of interest. There is no significant difference between the MST samples with and without defect-etch removal. Note that if random pyramids were used as the surface texture, an additional anti-reflection coating would be used, which would make this difference even smaller.

The loss in current density due to reflection losses (front surface reflection and secondary escaped reflection losses) were calculated and shown in Table I. Before lamination, the MST samples (with DRE) have a clear advantage over the random pyramids in terms of direct front reflectance loss, with a gain in current density of approximately 3.4 mA/cm^2. After lamination, however, the gain in current density, due to applying MST (with DRE), reduces to approximately 1 mA/cm^2, which is nevertheless still a significant value. However, in a real device an ARC would be applied on top of the random pyramids, which could make these apparent improvements even smaller. The MST samples exhibit the highest implied photocurrent beyond 41.5 mA/cm^2 even after encapsulation without any ARC.

Table I. The losses in current density due to direct front reflection loss and front escape loss are summarised in samples with different surface structures, namely, random pyramids texture (RPT),

modulated surface texture (MST) and MST with defect-removal etch (DRE), before lamination and after lamination

	Front reflection loss [mA/cm^2]	Secondary escape loss [mA/cm^2]	Implied photocurrent [mA/cm^2]
Before lamination			
RPT	5.18	2.05	38.67
RPT + MST	0.39	2.23	43.28
RPT + MST + DRE	1.80	2.06	42.04
After lamination			
RPT	3.41	1.62	40.87
RPT + MST	2.10	1.66	42.2
RPT + MST + DRE	2.48	1.52	41.9

2.3 MST passivation quality evaluation

The main challenge of applying MST in real devices is the difficulty in achieving high quality passivation with low surface recombination velocity. While the defect-removal etch removes the defects induced in the silicon due to the RIE process, the surface structures still possess high aspect ratios and sharp features which may be challenging to deposition techniques other than, for e.g., atomic layer deposition.

The passivation quality on the MST surfaces, achievable with intrinsic hydrogenated amorphous silicon (i-a-Si:H) passivation layer matching with a typical heterojunction IBC process, was evaluated. Wafers with double-side random pyramids surface texture were used as references, as depicted in the experimental split matrix in Figure 5. Both sides of the wafer were passivated using i-a-Si:H layer deposited by plasma-enhanced chemical vapour deposition (PECVD). In order to evaluate the effect of DRE process on the surface texture, three different dipping times are considered. After passivation of both surfaces, the minority carrier lifetime is measured, using quasi-steady-state photo-conductance (QSSPC).

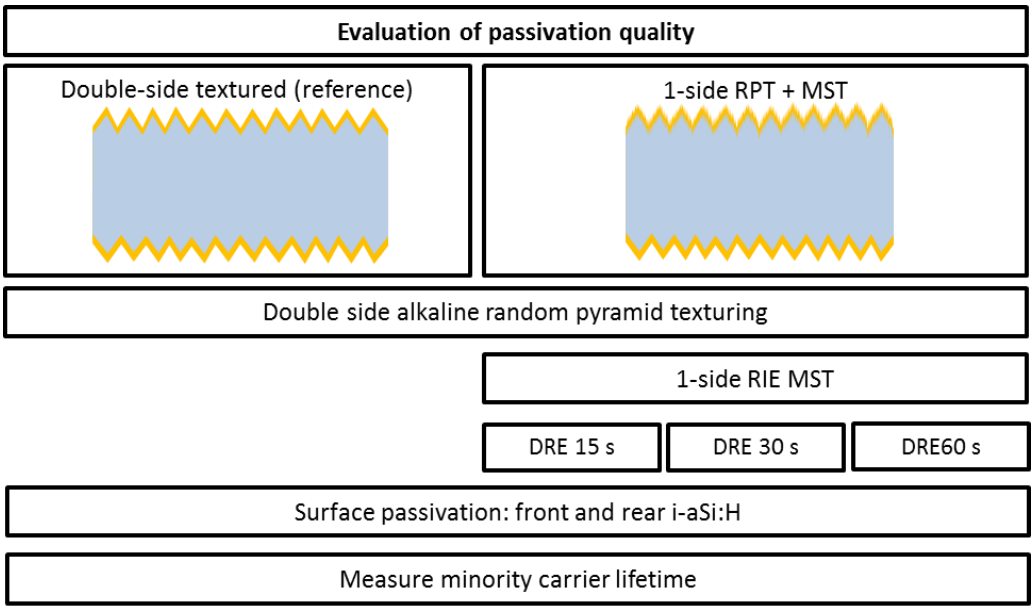
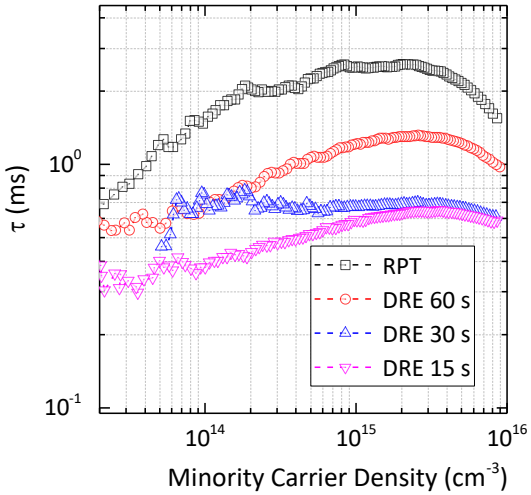


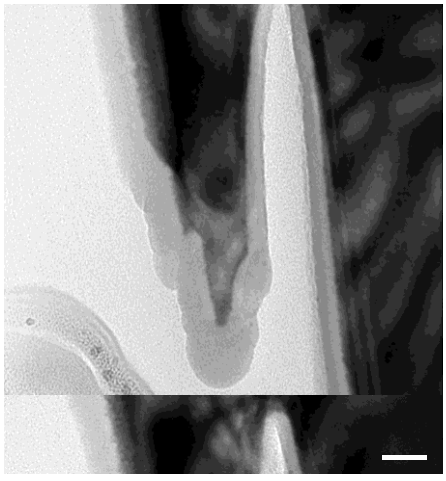
Figure 5. Experimental matrix to evaluate the passivation quality of samples with different surface textures: random pyramids surface texture and modulated surface texture (MST).

The injection-level dependent effective minority carrier lifetimes, measured on wafers with front RPT and MST, are plotted in Figure 6a. The effective lifetime is function of the bulk lifetime of the wafer and the surface recombination velocity at the interfaces. Since it is assumed that the bulk quality of the witness wafer used in this study are similar, and the texturing processes applied on them should not affect the bulk material, the bulk lifetimes are expected to be approximately similar. Moreover, high quality float zone wafers with high bulk lifetimes are used. Thus, the effective lifetime is mainly limited by the surface passivation quality. Accordingly, any variation in the effective lifetime is attributed to the changes on quality of the surface passivation. Additionally, the defects created on c-Si during MST process can be removed by dipping the samples on DRE solution (Ingenito et al., 2015). Thus, this passivation study also explore the effect of DRE time.

Using the standard i-a-Si: H recipe for passivation of textured pyramids, MST lifetime results are below 200 µs (not shown). However, after evaluating plasma deposition competitive mechanisms (i.e. best trade off of mass transport and surface reaction) during chemical vapour deposition (CVD), the plasma parameters were re-calibrated. With this deposition conditions, the effective lifetime of MST samples increased to more than 500 µs as Figure 6a indicates. The effective lifetime of the witness wafer (RPT) at the injection level of 10^{15} cm^{-3} is 2.6 ms (implied V_{oc} iV_{oc} = 725 mV). Results demonstrate a clear difference for different DRE times applied. Indeed, at 10^{15} cm^{-3} injection level, the effective lifetime is 591 µs (iV_{oc} = 692 mV), 668 µs (iV_{oc} = 694 mV) and 1.22 ms (iV_{oc} = 715 mV) corresponding respectively to 15, 30 and 60 s of dipping time of the samples in DRE solution. According to these results, 60s DRE time allows MST samples to reach the lowest recombination losses thanks to the conformal deposition of i-a-Si:H layers on nano-roughness surfaces shown on the transmission electron microscopy (TEM) image in Figure 6b. Such a conformal layer is achievable under proper plasma process conditions as described in (Procel et al., n.d.).



a)



b)

Figure 6. a) Effective minority carrier lifetimes measured on wafers with random pyramids texture (RPT) and modulated surface texture MST with different defect-removal etch (DRE) time. b) Transmission electron microscopy (TEM) image confirming conformal deposited i-a-Si:H on top of MST (Procel et al., n.d.).

To assess the effect of DRE time on reflectivity losses after i-a-Si:H passivation, reflectance curves are reported in Figure 7. Indeed, no significant changes (less than 0.5% - see Figure 7b) on reflectance are observed. Low reflectivity and recombination losses are achieved concurrently by MST sample dipped 60 s on DRE solution exhibiting the highest potential for achieving high J_{sc} and reduced recombination losses concurrently.

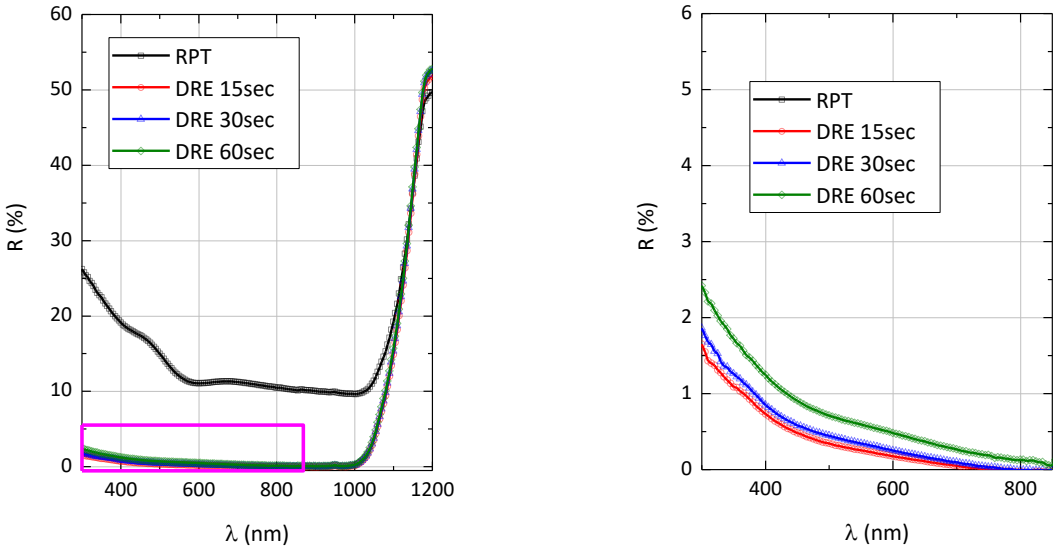


Figure 7. a) Measured reflectance measured different surface textures: random pyramids texture (RPT), modulated surface texture (MST) and MST with defect-removal etch (DRE). b) Inset of reflectance curve for different DRE time: 15 s, 30 s, and 60 s. (Procel et al., n.d.)

It is worth noting that the thickness of the passivating i-a-Si:H layer changes from 20 nm on sides to 50 nm on valley of nano-cones (see Figure 6b), thus indicating that there is still room for further optimization if measurements on final IBC devices confirm a considerable amount of parasitic absorption losses on i-a-Si:H. Besides, the potential of passivated MST is demonstrated in terms of low recombination losses (1.22 ms as effective lifetime and 715 mV as iV_{oc}) and low reflective losses (3.86 mA/cm^2), anticipating the potential of MST to achieve J_{sc} > 41.5 mA/cm^2.

3 Risks and interconnections

3.1 Risks/problems encountered

No risks or problems were encountered for this work.

3.2 Interconnections with other deliverables

This deliverable is related to the following deliverables/milestones/tasks:

- Task 5.2:
  - "Investigation of light management"
  - In task 5.2, light management texture and technique are investigated, including experimental results from WP3: advance texturing surfaces.
- Deliverable D5.2:
  - "Light management scheme allowing Jsc > 42 mA/cm^2 (interlinked to D4.3)"
- Task 7.3:
  - "Liquid encapsulation process"
  - As part of task 7.3, liquid encapsulation process is evaluated on advanced textured surfaces.

4 Conclusions

An advanced surface texturing scheme called modulated surface texturing (MST) was evaluated by comparing the optical properties and passivation quality with the standard random pyramids texturing scheme. MST consists of nano-cones superposed on random pyramid surface texture. Such a surface has a broad-band anti-reflective property, with the potential to reduce the front surface reflection losses significantly. Moreover, with such a texture, there is no necessity to use an additional anti-reflection coating layer during device fabrication.

Nano texturing process is carried out by reactive ion on a mixture of SF_6 and O_2 gases. After achieving the nano-roughness etching regime, the minimum etching process time to reach almost a perfect light-in coupling in wavelength range of interest was found to be 5 min.

Then, based on the optimized process, a comparison of wavelength-dependent reflectance of MST and RPT samples was carried out. Before lamination, results showed that the reflection losses can be reduced by up to 3.4 mA/cm^2. However, after lamination, this advantage is reduced to 1 mA/cm^2. The MST samples exhibited front reflection loss below 4% and also the highest implied photocurrent beyond 41.5 mA/cm^2 even after encapsulation without any ARC.

Finally, aiming at including MST process for IBC-SHJ devices, the passivation quality of MST surfaces using i-a-Si:H was evaluated in terms of effective lifetime. Standard i-a-Si:H recipe used to passivate RPT showed a poor passivation. Then after a calibration of plasma conditions, effective lifetime beyond 500 µs was achieved thanks to an i-aSi:H conformal layer. Under these conditions, the effect of DRE time on effective minority carrier lifetime was evaluated exhibiting promising values as 1.2 ms for 60 s DRE time, and 715 mV as iV_{oc}. The impact of passivated MST for different DRE time was also evaluated demonstrating that there are insignificant changes on reflective losses between 15 s and 60 s DRE time. Therefore, MST with 60 s DRE concurrently exhibits reduced reflectivity losses and recombination losses anticipating the potential of MST to achieve J_{sc} > 41.5 mA/cm^2 in IBC device level.

5 References

Ingenito, A., Isabella, O., & Zeman, M. (2015). Nano-cones on micro-pyramids: modulated surface textures for maximal spectral response and high-efficiency solar cells. *Progress in Photovoltaics: Research and Applications*, *23*(11), 1649–1659. https://doi.org/10.1002/pip.2606

Jansen, H., Gardeniers, H., & De Boer, M. (n.d.). The black silicon method: a universal method for determining the parameter setting of a fluorine- based reactive ion etcher in deep silicon trench etching with profile control Related content A survey on the reactive ion etching of silicon in microtechnol. *Journal of Micromechanics and Microengineering*. Retrieved from http://iopscience.iop.org/article/10.1088/0960-1317/5/2/015/pdf

Procel, P., Ozkol, E., Medlin, R., Sutta, P., Isabella, O., & Zeman, M. (n.d.). Effective Passivation of Black Silicon Surfaces via PECVD Grown Conformal a-Si:H Layer . to be submitted.